

Application No.: 09/784,087
Art Unit: 2871

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On page 13, paragraph beginning on line 14:

ay Next, as shown in Figure 6C, using the passivation layer 112 as a mask, the exposed doped amorphous silicon layer 154 is etched away. The exposed portions of the drain electrode 116 and data pad 120 are also etched away such that the drain contact hole 117 and the data pad contact hole 122 are formed. Since the drain electrode 116 and the data pad 120 are comprised of a metal that can be dry-etched it is possible to etch both the metal and the doped amorphous silicon layer 152 together. The drain contact hole 117 and the data pad contact hole 122 expose inner side portions of the drain electrode 116 and the data pad 120, and planar portions of the gate insulating layer 150.

In the Claims

Please amend the claims as follows (A marked-up version of the amended claims is attached):

- as
LSP
1. A liquid crystal display device comprising:
 - a substrate;
 - a thin film transistor including a gate electrode, a source electrode, and a drain electrode on the substrate;
 - a pixel electrode electrically connected to the drain electrode;
 - a data line electrically connected with the source electrode;
 - a first insulating layer, a pure amorphous silicon layer, and a doped amorphous silicon layer sequentially layered under the data line;
 - a data pad at one end of the data line; a gate line electrically connected with the gate electrode; and
 - a gate pad electrode at one end of the gate line;
- wherein the gate pad electrode is formed directly on top of the first insulating layer,
wherein the first insulating layer includes an opening that exposes a portion of the gate

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as
cont

line, and wherein the gate pad electrode electrically contacts the exposed portion of the
gate line and overlaps the first insulating layer.
